IN THE DRAWINGS

The attached sheets of drawings include changes to Figs. 6A-6D and 7A-7C. These sheets, which include Figs. 6A-6D and 7A-7C, replace the original sheets including Figs. 6A-6D and 7A-7C.

Attachment: Replacement Sheets

REMARKS/ARGUMENTS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-6 are presently pending. Claims 1 and 2 are amended by the present amendment. No new matter has been added.

In the outstanding Office Action, the Abstract was objected to as being too long; Figs. 6A-6D and 7A-7C were objected to; Claims 1-6 were rejected under 35 U.S.C. § 112, second paragraph; and Claim 1-6 were rejected under 35 U.S.C. § 103(e) as being unpatentable over U.S. Patent No. 6,370,768 to Itabashi (hereinafter "Itabashi").

Regarding the objection to the Abstract, a replacement Abstract of less than 150 words has been provided herewith. Therefore, Applicants respectfully submit that the objection to the Abstract should be withdrawn.

Regarding the objection to the drawings, replacement sheets 6 and 7 of the drawings containing Figures 6A-6D and 7A-7C are submitted herewith. The replacement sheets have been designated as Background Art. Thus, Applicants respectfully submit that the objection to the drawings should be withdrawn.

Regarding the rejections under 35 U.S.C. § 112, second paragraph, the cited phrases of Claims 1 and 2 have been amended to more clearly recite the claimed invention. Thus, Applicants respectfully submit that the rejection of Claims 1-6 should be withdrawn.

Applicants respectfully traverse the rejection of Claim 1-6 under 35 U.S.C. § 103(a) as unpatentable over Itabashi.

Amended Claim 1 is directed to a method of manufacturing an electronic part comprising a conductor film, a lower conductor layer, and an insulating member sandwiched between the conductor film and the lower conductor layer, for connecting the conductor film and the lower conductor layer by conductor portions. The method includes:

> forming a plurality of opening holes, each having said lower conductor layer as bottoms, through the conductor film and the insulating member from said conductor film side,
>
> growing metal plating layers, as conductor portions from each of the bottoms of said opening holes, from said lower conductor layer as an electrode,
>
> growing metal plating layers on the upper surfaces of said conductor film and said conductor portions with said conductor film and said conductor portions as electrodes after said conductor portions are formed in the respective plurality of opening holes by growing said metal plating layers so as to contact said metal plating layers with said conductor film, and to increase area for growing said metal plating layers and reduce current density per unit in said metal plating layers, so as to lower growing speed of said metal plating layers, to thereby form said conductor portions in said opening holes, and forming a thickness enough to form an upper conductor layer.

Support for the present amendment is found at least at page 10, line 4-24, of the specification.

Applicants respectfully submit that Itabashi fails to disclose or suggest each feature of Claim 1. For example, it is respectfully submitted that Itabashi fails to describe growing said metal plating layers so as to contact said metal plating layers with said conductor film, and to increase area for growing said metal plating layers and reduce current density per unit in said metal plating layers.

Itabashi describes uniformly filling via holes (a.k.a., "vias") in a circuit board using electroless plating, which is a method that does not use electrodes to fill the via holes. The uniformity of the level of fill metal in the vias of Itabashi is obtained by applying a potential higher than the potential of the electroless plating to the conductor on the surface when filling the via holes by electroless plating.[1] Thus, according to the method of Itabashi, "when the upper end of the plating metal contacts the semiconductor, the plating reaction is stopped, and the thickness of the plating metal does not increase anymore."[2]

The Office Action also cites column 11, lines 52-61, of Itabashi, as disclosing

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[1] See Itabashi at abstract.
[2] See column 7, lines 8-11 of Itabashi.

growing or forming a metal plated layer on the entire surface including the via hole and the upper conductor film by an electroplating process.

According to the process steps of Itabashi, as characterized in the Office Action, the via is filled by an electroless plating process until the level is high enough to contact the surface conductor, and an electroplating process is then used to add a metal layer to the surface conductor as well as to the surface of the via.[3] Thus, when the electroplating process of Itabashi begins, the surfaces of both the via and the surface conductor are being electroplated simultaneously. Therefore, when electroplating begins, after the electroless process of Itabashi, the current density at the conductive surface depends on the total combined surface areas of the via and the surface electrode. Since the area being electroplated by Itabashi does not increase once it begins, the current density in the method of Itabashi is not reduced, and the growing speed of the metal plating layers is not lowered. Therefore, Itabashi fails to suggest reducing a current density.

Thus, Applicants respectfully submit that Itabashi fails to teach or suggest "growing said metal plating layers so as to contact said metal plating layers with said conductor film, and to increase area for growing said metal plating layers and reduce current density per unit in said metal plating layers, so as to lower growing speed of said metal plating layers," as recited in amended Claim 1.

For an additional reason, distinct from the reasons given above, Applicants traverse the rejection of Claim 1.

The cessation of via fill metal deposition in Itabashi depends on the reaction between the via fill metal and the conductor on the surface.[4] Consequently, Applicants respectfully submit that in the electroless plating process of Itabashi, the level of the via fill metal is raised to a point just **below** the conductor on the surface because the electrical potential of the

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[3] See Office Action at page 5.
[4] See Itabashi at col. 8, l. 27 to col. 9, l. 5.

surface conductor will cause corrosion of the via fill metal when the fill metal contacts the surface conductor.

Thus, Applicants respectfully submit that Itabashi fails to teach or suggest "growing said metal plating layers so as to contact said metal plating layers with said conductor film," as recited in amended Claim 1, for that distinct reason in addition to the reasons noted above.

Accordingly, it is respectfully submitted that independent Claim 1 (and all associated dependent claims) patentably defines over Itabashi.

Independent Claim 2 recites limitations analogous to the limitations in Claim 1 and has been amended in a manner analogous to the amendments to Claim 1. Thus, Applicants respectfully submit that, for reasons stated above, Claim 2 (and all associated dependent claims) also patentably defines over the cited reference.

Consequently, in view of the present amendment and in light of the above discussion, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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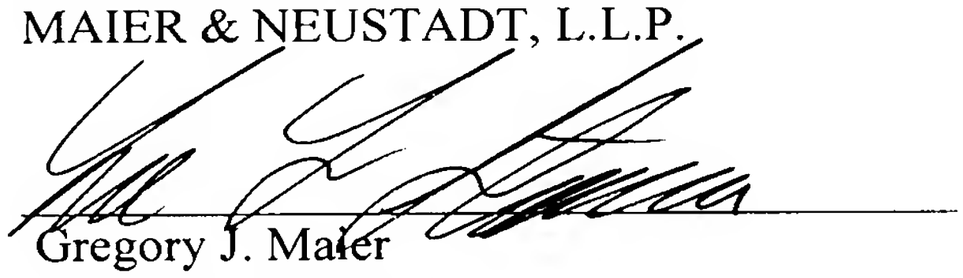

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